

Appl. No. 09/702, 462
Amdt. dated May 19, 2004
Response to Office Action of March 17, 2004

Amendments to the Specification:

Rewrite the title from the previously amended title in the Response to Office Action mailed October 10, 2003 as follows:

**MICROPROCESSOR WITH AN INSTRUCTION ~~SEQUENTIALLY~~ ADJACENT
IMMEDIATELY NEXT TO A BRANCH INSTRUCTION FOR ADDING A CONSTANT TO
A PROGRAM COUNTER**

Insert the following new paragraph at page 6, after line 29:

Figure 6C is a flow chart illustrating a subroutine call B func with a return address computed using an ADDKPC instruction, a MV instruction inserted in a delay slot, and a NOP instruction;

Figure 6D is a flow chart illustrating the instructions of Figure 6C re-ordered to absorb the NOP instruction, according to an aspect of the present invention;

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Rewrite the paragraph at page 28, lines 13-29 as follows:

A compiler can embody an aspect of the present invention to use an ADDKPC instruction to re-order a sequence of instructions to place the ADDKPC in such a way that the parallel NOP field is used to encode any NOPs in the delay slot of a calling branch instruction. This is done to save code size. For example, the following instruction sequence shown in Figure 6C and described below:

B	func	; call a subroutine
ADDKPC	R0,B3	; calculate return address
MV	A10,AA4	; move parameter
NOP 3		; three NOPs for the remaining delay slots

would be re-ordered as shown in Figure 6D and described below ~~like this~~ to "absorb" the NOP

B	func	<u>; call a subroutine</u>
MV	A10,A4	<u>; move parameter</u>
ADDKPC	R0,B3,3	; provides three virtual NOPs for remaining delay slots